PRX205

SYSTEM MANUAL

DB-A 7400e-3

Issue: a

Philips' Telecommunicatie Industrie B.V.

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1. INTRODUCTION

1.1. General

The processor controlled exchange PRX/A is a fast and reliable miniaturised telephone switching system that operates under the control of duplicated stored-program processors. The system is designed for use in applications ranging from simple local terminal exchanges or trunk exchanges to any combination of subscriber, transit or tandem exchange systems. The PRX/A can be economically applied to initial traffic volume requirements as low as 100 Erlangs and extended, on-line, to capacities of up to several thousand Erlangs without disturbing the existing equipment or service.

The PRX/A system employs glass-sealed reed relays as crosspoints in a multi-stage linked Switching Network. These electrically latched, metallic reed switches were chosen to ensure high quality speech transmission. The system has two types of terminating equipment. Junctors for analogue signalling systems consists largely of electronic components, completed by reed relays and mercurcy wetted relays for signalling purposes. The terminating units for digital trunk lines comprise mainly LSI components.

The system has a Central Control Complex which consists of up to three Central Control Units. Each Central Control Unit is a pair of general purpose data processors, designed for on-line operational control.
Only one of the three Central Control Units interfaces with the Switching Network and performs the input output functions, the other two are used for call processing. A processor belonging to the first type is called main processor, and the other ones are called secondary processors.
The number of pairs of processors in any exchange will depend on the traffic requirements of that exchange. The Central Control Complex carries out the common control functions associated with recognition, identification and routing of incoming calls, selection of suitable speech paths through the Switching Network and maintenance of a continuous record of the network status.

In the PRX/A system, functions such as timing and some of the logic previously performed, in electro-mechanical switching systems, by electro-mechanical relays have been taken over by software so that the trunk circuits contain only essential transmission and signalling related components. This has produced a reduction in both the size and the cost of trunk and service circuits. The system is fully compatible with existing electro-mechanical switching systems, both private and public, and can be installed in networks using any numbering plan.

PRX/A exchanges are available in two or four wire versions and can be used for local and trunk switching. The flexibility of stored program control enables new subscriber facilities and the intermixing of signalling systems and codes, alterations of routing codes, the read-out of metering data and the blocking/unblocking of subscriber facilities to be carried out simply and quickly.

In addition to the control of the operation of the telephone switching network, the Central Control Complex can perform the functions required for administration and technical supervision of the centre including call accounting, measurement of traffic statistics, automatic routine testing and the display of equipment and line status. The maintenance and administrative functions for a number of exchanges may be centralized and controlled from one location which acts as an operational and maintenance centre for a certain area.

1.2. Basic System Description

The smallest configuration of a PRX/A system comprises a Switching Network, Control Channel and interface equipment, utility and integral test equipment and a Central Control Unit (see diagram 100).
The Central Control Complex can be extended in memory capacity as well as processing capacity to provide a higher grade of service (memory) or a higher traffic capacity (processing) (see diagram 101).
The five possible combinations of Central Control Units, Memory Switch and Central Memory are listed in the table below.

Combination	Number of CCU's	Memory Switch (0,1)	Central Memory (0,1)
1	1	-	-
2	1	-	1
3	1	1	1
4	2	1	1
5	3	1	1

In combination 2 and 3, the Central Memory is used as an extension memory. A Memory Switch is necessary for reliability reasons when the capacity of the extension memory exceeds 256K words of 18 bits. By means of this Memory Switch a configuration cross is introduced between each processor of the pair and each Central Memory, in this way increasing reliability.
In combination 4 and 5, the Central Control Unit 0 is the heart of the Central Control Complex interfacing with the

Control Channel and interface equipment and distributing software tasks to the Central Control Units 1 and 2 via the Central Memory. Processors of Central Control Unit 0 are called main processors and processors of Central Control Unit 1 and 2 are called secondary processors.

Note:

When Central Control Unit 0 is performing the function of Central Control Complex (combination 1,2,3) please read Central Control Unit where Central Control Complex is written.

The Switching Network consist of all the equipment required to build up telephone connections. It may have various configurations of line terminating equipment and link blocks, depending on the traffic handling requirements of the exchange. The network can build up connections, under control of the CCC, for incoming, outgoing, transit and local calls and it can handle various signalling methods, such as multi-frequency code, hook signalling types etc. For digital trunk lines a digital version of an appropriate signalling type can be used. The Switching Network can also provide a number of 'services', such as information tones and announcement facilities.

The utility equipment consists of a Visual Display Unit, a Hard Copy Printer and a number of Cartridge Tape Units. The VDU and HCP are used for man-machine communication, the CTU-('s) are available for loading the system and for the dumping of large quantities of data, e.g. subscribers meter data. The integrated test equipment is available for testing the operational telephony equipment in the Switching Network and for testing the subscriber lines.

The Control Channel and interface equipment consists of terminating equipment for the Control Channels (CCH), Subsystems and Peripheral Control Subsystems. The Control Channel and Subsystem Terminal (CST) is an interface between the duplicated Control Channel (CCH 0 and 1) and a group of Subsystems. There are a number of subsystem types, such as Testers (TR), Slow Drivers (SD), Fast Drivers (FD), Markers (MR) and Subsystems for controlling utility equipment etc. Testers are used to monitor all telephony equipment (for analoque lines) to detect changes in their status. Markers are used to energise and de-energise the cross-point reed relays in the link blocks and Drivers are used to control the analogue telephony units. These subsystems are controlled by Central Control Unit 0 and all commands and data transfers are passed via the CCH and a CST.
The Control Channel Terminal (CCT) is an interface between the Control Channels (CCH 0 and 1) and the Peripheral Control

Subsystems (PCS). The CCT may be regarded as a type of CST and it has a similar interface with the CCH. The PCS is used to control Peripheral Modules in the Switching Network, which can be used, for example, as terminating equipment for digital trunk lines. Communication between a PCS and a number of Peripheral Modules (PM) is possible via Peripheral Channels. These channels consist of serial 2 Mbit/s busses for the transmission of commands, signalling and housekeeping data etc.

The Central Control Complex is responsible for the establishment, supervison and release of the telephone connections. The Central Control Complex achieves this by:

a. Initiating scanning and polling procedures, to investigate new signals arriving in the Switching Network, processing the information received and modifying the Switching Network accordingly.

b. Controlling the system configuration to ensure a reliable service.

c. Obeying commands, received from the operator via the utility equipment.

d. Carrying out administrative tasks.

The utility equipment is provided to allow the man/machine communication that is necessary for operational and maintenance purposes. It is via this equipment that, detailed information about the service condition of any hardware item is given, manually controlled tests of the system can be carried out and various alarm signals pass when any part of the system is defective.

1.3. Documentation

The available documentation, associated with the PRX/A system is fully listed in DB-A 7583, the "Organisation of Operation and Maintenance Documentation". The documentation consists of a number of publications divided into five groups.

a. The Hardware Manuals consist of all the publications providing the functional and physical descriptions of the individual hardware equipment in the system.

b. The Maintenance Tools Manuals consist of all the publications providing the descriptions of equipment available for aiding the testing and maintenance of the system.

c. The Office Data Manuals consist of all the publications, in computer print out form, giving the project specifications e.g. inter-cabinet wiring.

d. The Operations Manuals consist of all the publications providing the procedures for testing, operating and maintaining the system.

e. The Explanatory Manuals are a collection of publications which provide a guide to the reader for the interpretation of specific documentation, e.g. computer listings.

2. PROJECT SOFTWARE AND INITIATION OF THE EXCHANGE

2.1. Production of Software for an Exchange

For each individual exchange, a subset of program components must be selected to provide the facilities required in that particular exchange. The data structures upon which these program components operate must reflect the actual or planned dimensions of the exchange. The production tool used to generate these programs and data structures is referred to as the Project Generator System. The exchange description in telephony terms, is read into the Project Generator System and it outputs, in a computer loadable form, load tapes, some semi-permanent data tapes, service condition data tapes, test tapes and various system documents. A simplified lay-out of the system is given in figure 2.1.

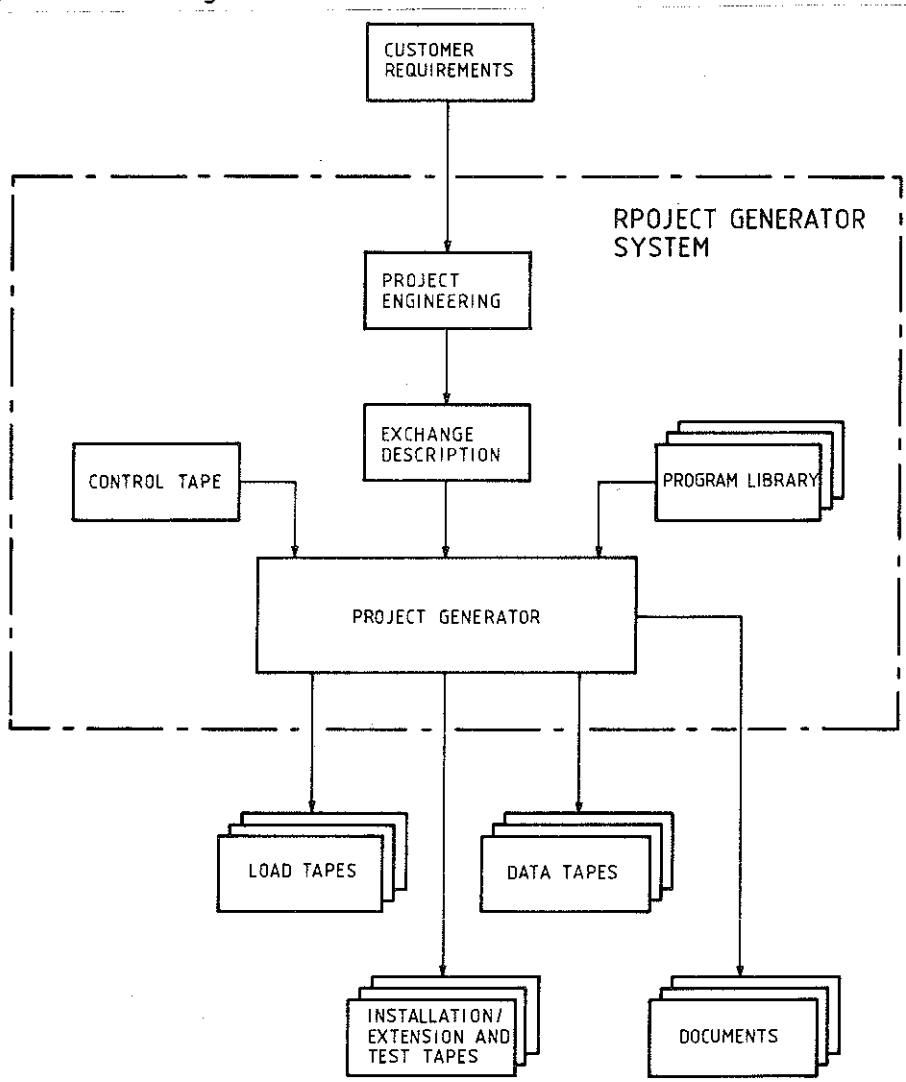

Fig. 2.1. Simplified Diagram of the PGS

2.1.1. Load Tapes and Data Tapes

For each exchange a number of load tapes are provided, which are the output from the Project Generator System and contain all information which is necessary to make the Central Control Complex (CCC) operational. The number of load tapes depends on the configuration of the CCC, viz. for each CCU separate load tapes are required, in addition to a number of common ones. For an exchange with 3 CCU's the following (program) loadtapes are available on cartridges:

- Loadtape PME (CCU0) and loadtape CME;
- Loadtape PME (CCU0, this is an additional tape);
- Loadtape PME (CCU1);
- Loadtape PME (CCU2).

In addition to these load tapes a number of data tapes are available (also on cartridges). These contain the following data groups:

- Installation data;
- Operation data;
- Restricted data;
- Transition data;
- Administration data.

2.1.1.1. Contents of the Load Tapes

The loadtapes contain the resident operational programs for the system and the associated data, i.e. the permanent (fixed) data and frames for variable data (see also section 4.2.4.1.). For each of the PME loadtapes, the Project Generator System selects all program and data modules which are necessary for the particular CCU (main or secondary CCU). These modules are selected from the program module and data module files of the support system. It is possible that a program module is selected for each of the PME load tapes. This will be the case for "universal" programs, which can be used in each CCU. Other modules are exclusively for a particular CCU (CCU0,1 or 2). An important factor in the selection process of the modules are the functional differences of the CCUs.
Functions exclusively for the Main CCu are:

- I/O control, including scanning mechanism control;
- Configuration Management and Maintenance;
- Handling of operational services, such as overlay program and administration data handling.

The functions of the secondary CCUs are "common" functions, which can be executed by any CCU, including CCU0.

Examples of these functions are:

- Call Processing;
- Interrupt handling (although not every CCU can receive all kinds of interrupts);
- Error handling (although for secondary CCU's restricted to errors occurring in the "own" processors and PME's).

The CME loadtape contains information which must be accessible by any processor. The CME may also contain information which is to be used by one CCU exclusively. Each of the three possible CCU's may have their extension to their private memory in a part of the CME. The majority of the CME data however is available for all CCU's. The following main groups can be distinguished:

- Data structures and definitions for the operational data and for other kinds of data;
- Facilities (data structures) for communication between main and secondary processors;
- Periodic tests, which can be executed when the system is operating;
- Definitions and structures of the Overlay Area, defining the memory areas which can be used for loading the overlay programs and the connection (link) facilities for these programs.

The loadtapes are stored on a number of cartridges. This number dependent upon the size and requirements of the exchange. For a group of exchanges which have common characteristics, e.g. because they belong to the same project, the loadtapes are standarized as far as possible. When a "standard load tape" is used, an additional tape is used to modifiy and extend the memory contents so that the specific requirements for the particular exchange are fulfilled.

2.1.1.2. Contents of the Data Tapes

The data tapes contain the following main categories:

a. Installation data.
This cartridge contains semi-permanent data, e.g.

- Junction group data;
- Test inlet data;
- Unit type definitions.

b. Operation data.
This category comprises programs and data which are to be used for load and test procedures. For example:

- Unit tests;
- Subsystem tests;
- X-ray programs;
- System loader;
- Overlay programs.

c. Restricted data.
Restricted data can be prepared on request of the administration when it is required that only authorized personel have access to certain information or functions.

d. Transition programs and data.
This information is stored on a cartridge which is to be used when the exchange is to be modified or extended.
The cartridges contain programs and data which are required to enable the transition from the old to the new requirements. (i.e. the transition from and old to a new project-group). During an extension or modification process one side of the CCC is taken off-line. The new programs and data are stored in the off-line memories. The cartridges contain also routines which enable retrieval of the operational data in the on-line memories and storage of this information in the off-line side, so that when the change is effected and the off-line side becomes operational, the memory contents is up to date.

e. Administration data.
This group consists of data which is to be provided by the administration. It comprises:

- Basic subscribers data;
- Subscribers facility data;
- Digit and routing analysis data;
- Tariff and Call charging data.

2.2. Initiation of the Exchange

Once the hardware for an exchange has been installed and tested, the programs and data must be loaded into the private and central memories to enable the system to function operationally. A hardware load channel is manually selected on control panels using the procedures described in the Operations Manual. The load tapes are then read from the tape device and stored in the memories. Further manual actions are carried out at the Processor Control Panel, System Control Panel and Mas-

ter Switch Unit to allow the loaded side of the CCC to "recover". The processors now run under the control of the stored programs, but, however, they fulfil no useful purpose until the semipermanent data and service condition data have been loaded. Firstly the overlay programs are loaded into a special area of the memory and they are initiated from the input/output device to supervise the loading of the semi-permanent data. Next the equipment outside the Central Control Complex (interface and Switching Network Equipment) must be put into operation. This is achieved by setting the equipment status record, held in the memory, to the "in-service" condition. A resident program (included in the load tapes) is initiated from the input/output device to supervise the loading of the service condition tapes which provides the correct equipment status record. Now the system is operational (i.e. information is received from test points throughout the system and this information is processed and responses produced).

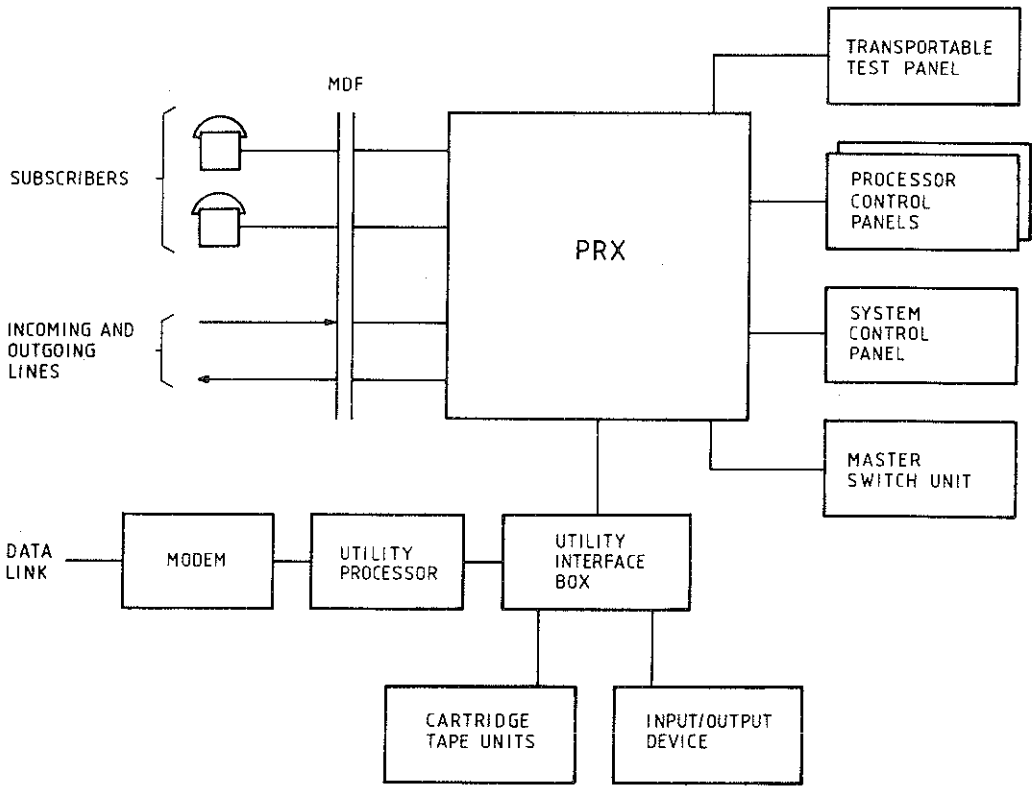

Figure 2.2. Simplified Block Diagram of the Exchange

3. HARDWARE DESCRIPTION

Diagram 102 is a block diagram showing a general lay-out of the equipment in an exchange. Diagram 103 shows the connections between the hardware components of the system in the smallest configuration in more detail, and diagram 104 shows the Central Control Complex in maximum configuration.

3.1. Switching Network (see diagram 105)

The main purpose of the Switching Network (SN) is to provide paths through the exchange between telephony lines, or between equipment in the exchange and an external line.
The network consists of two link networks and a number of telephony units. Telephony units are either line terminating units or units which provide other "services" such as the handling of tone detection or generation. There are four basic types of terminating units, or "junctors" which are the following ones:

- A-junctors (AJ); for originating traffic;
- B-junctors (BJ), for terminating traffic;
- Incoming Trunk junctors (IT), for incoming traffic;
- Outgoing Trunk junctors (OT), for outgoing traffic.

The AJ and BJ units are used for low density traffic lines of subscribers' sets or (small) PABXs. They are connected to the lines via the Line Link Network, which concentrates the lines, to increase the circuit efficiency. Lines with a high traffic density, connected to a PABX, may be terminated by a special version of the above mentioned junctors: AJI and BJO (for incoming and outgoing traffic respectively).
Trunk lines from and to distant public exchanges are terminated by IT and OT units. Dedicated telephony units are available for tone handling purposes. These units are the senders (S) and receivers (R), which are used for signalling systems employing, for example, keytone or MFC signals. The telephony units of the A-side of the exchange (AJs, ITs and Senders) are connected to the B-side units (BJs, OTs and Receivers) via the Trunk Link Network. Each A-side unit can be connected with each B-side unit, with a very low blocking probability.
The telephony units in the Switching Network are monitored and controlled by means of the subsystems, which are a part of the interface with the CCU. There are two methods of interfacing between telephony units and subsystems. The majority of units are monitored by Testers and they can receive commands via Slow or Fast Drivers. Each unit may have one or more test points and drive points and they each have a direct interface with the subsystems. For current developments a different

method can be used. When this method is used, a group of up to 32 units is assigned to a Peripheral Module Group (PMG). A PMG may have one or more Peripheral Module (PM) connections which provide the interface between the PMG and a subsystem. The interface is a 2 Mbit/s serial bus system, called the Peripheral Channel. The subsystem, which combines the functions of a Tester and a Fast Driver, is the Peripheral Control Subsystem (PCS). The paths through the link networks LLN and TLN, are switched through and released by means of subsystems, referred to as Markers (MR).

3.1.1. A-Side Junctors

All inputs to the Switching Network must be supervised and the lines controlled. This is achieved by connecting telephony units (or junctors) to the lines for the duration of a call. All signals and speech relating to the call will pass through the junctors, incoming traffic being supervised by incoming trunk junctor circuits (ITs), low density originating traffic being supervised by A-side junctor circuits (AJs) and high density originating traffic (e.g. some P(A)BXs) being supervised by A-side junctor circuits directly connected to a subscriber line (AJIs).
When an AJ is needed, a path between the subscriber line and an idle AJ is established and the AJ is seized. The AJ can then signal events (any relevant change of line conditions) to the CPU by changing a test point condition and it can receive commands (e.g. to send a tone) via the drive points. At the end of the call the LB-path and the junctor are released and the unit may be used for a next call. The AJI and IT operate in a similar manner. They are, however, permanently connected to the lines. When the line status changes, for example when the distant public exchange or PABX sends a seizure signal, this change is reflected by a change in the condition of a test point.
If an IT belongs to a PMG, the operation is similar, but the events and commands are transferred between the IT and the PCS by means of a byte transfer.

3.1.2. B-Side Junctors

All the outputs from the Switching Network must be supervised and again this is achieved by connecting all the output lines to junctors. The outgoing lines and high density P(A)BX lines are permanently connected to outgoing trunk junctor circuits (OTs) and B-side junctor circuits (BJOs) respectively, and the low density terminating lines are connected to

inlets of Line Link Blocks of which the outlets are connected to BJs (and AJs).
When a subscriber must be called, a free BJ is selected and connected to the subscribers line, via the LLN, and the BJ is connected to the A-side unit via the TLN. When the speech phase of the call has finished, the paths are released and the BJ becomes available for a new call.
BJOs and OTs are seized when a call must be made via the outgoing line to which they are connected. When they are not engaged in a call process they guard the outgoing line.
The B-side units are monitored and controlled in the same way as the A-side units, i.e. either by Testers and Fast or Slow Drivers or, if they belong to a PMG, via the PCS and a Peripheral Channel.

3.1.3. Line Link Network

The originating subscriber inputs carry low density traffic and, to be economical in use of telephony units and to increase circuit efficiency, the lines are concentrated by the Line Link Network (LLN). The junctors (AJ and BJ) are only connected to the lines when needed. The LLN consists of one or more blocks (LB), which are interconnected by means of a number of links.

The LB is a bi-directional, three stage network, each stage made up of a number of switches, connected together in such a manner that any LB inlet can reach any LB outlet.
The concentration factor of the LBs depends on the type of switches used in the switching stages. The inlet/outlet ratio ranges between 1:2 and 1:8. In general the number of AJs and BJs is approximately equal, giving a concentration factor twice as high as the LB inlet/outlet ratio. The AJ/BJ ratio, however, can be changed, when there is more traffic in one direction.

3.1.4. Trunk Link Network

Once the A-side junctors and the B-side junctors for a telephone connection have been established, the Central Control Complex has to find a path from one junctor to the other via the Trunk Link Network. The Trunk Link Network is a six stage switching network containing a number of Trunk Link Blocks (TBs). The Trunk Link Blocks into which the A-side junctors are connected are called TB-As and are used as expanders. The Trunk Link Blocks into which the B-side junctors are connected are called TB-Bs and they are concentrators.

Both TB-As and TB-Bs have three switching stages and the outlets of the TB-As are connected to the outlets of the TB-Bs. In principle the TB-A and TB-B can be seen as a mixing unit, which enables paths to be made from inlets on one side to all inlets on the other side.
The software maintains a record of the condition of all the switches in the Trunk Link Network, and it searches this record for an unengaged, serviceable path from the B-side junctor to an outlet on the TB-B. As an outlet of the TB-B is connected to a specific outlet on the TB-A, the software searches next for an unengaged, serviceable path from the A-side junctor to this outlet. Commands are then given from the Central Control Complex via a Marker to establish the paths found.

3.1.5. Receivers and Senders

To enable the PRX/A system to be used with more complex methods of signalling than the junctors can handle, such as keytone, multi-frequency code, etc., Receiver and Sender units are provided in the Switching Network.
Usually, the Receivers and Senders are required only for the reception and transmission of number information. Therefore to ensure an economical usage of both units, the Receivers are connected to certain inlets of the TB-B and the Senders are connected to certain inlets of the TB-A and the units are released when they are not needed.

The Central Control Complex keeps a record of the method of signalling used for each subscriber. When a Receiver (R) is required to decode an incoming signal, the Central Control Complex gives a command to a Fast Driver (part of the interface equipment, see paragraph 3.2.) to "seize" the required type of Receiver and a command to a Marker to connect a path through the TB to the appropriate A-junctor. The information decoded by the Receiver is passed to the Central Control Complex via a Tester.

The Senders are connected through the TB-A and TB-B to the OTs, BJs and BJOs when the other exchange uses one of the more complex methods of signalling. When the terminating subscriber's number has been received via the the A-side junctor, it is analysed by the Central Control Complex, a path is established between a free Sender (S) and the required B-side junctor, and the number information is given to the Sender. When the terminating exchange has received the information, the Sender and the path through the Trunk Link Block are released, and the Central Control Complex connects a speech path between the A-side junctor and the B-side junctor in the normal manner.

3.1.6. Primary PCM Multiplexer (see drawing 106)

The Primary PCM Multiplexer (PPM) is a type of Peripheral Module Group (PMG). The PPM interfaces between a 2048 kbit/s full duplex PCM line and the TLN. It contains a first order multiplexer and demultiplexer function, which handles the digital coded samples of 30 speech channels and of two additional channels.

The 32 channels of the PCM line are numbered from 0 to 31. Channel 0 is mainly used for PCM-group error signalling and for frame synchronisation of the PCM link. Channel 16 is mainly used for telephony signalling and for multiframe and error signalling. This channel carries the channel associated signalling of the 30 telephony channels (which are numbered 1... 15 and 17...31). The analogue channels are connected to the TB-A and TB-B, via an IDF. These channels can be used either for incoming or outgoing trunks, i.e. the PPM performs the function of up to 30 ITs or OTs. It is possible to use four or more channels for incoming lines and the remaining ones for outgoing lines at the same time (selection is possible in groups of 4 units).
The PPM has two Peripheral Module-connections, i.e. it interfaces with the PCS via two Peripheral Channels. The first Peripheral Channel is used for the Digital Trunk Interface circuits (DTI) of the PPM, which provide the line interface and handle the frame synchronisation and line group signalling. The second Peripheral Channel is used for telephone channel and multiframe signalling, which is transferred over the PCM link in time-slot (channel) 16, and it is used to guard and control the multiplexer and demultiplexer circuits (PMX).

The PPM is equipped with Conversion Junctor (CJ) circuits which establish the analogue to digital conversion (and vice versa) and may contain hybrid circuits, to provide 2-wire channel outputs or inputs. These CJs may have one or more attenuation pads, which can be switched in or out by sending commands to the PMX.

3.1.7. Tone Injection and Announcement Circuits

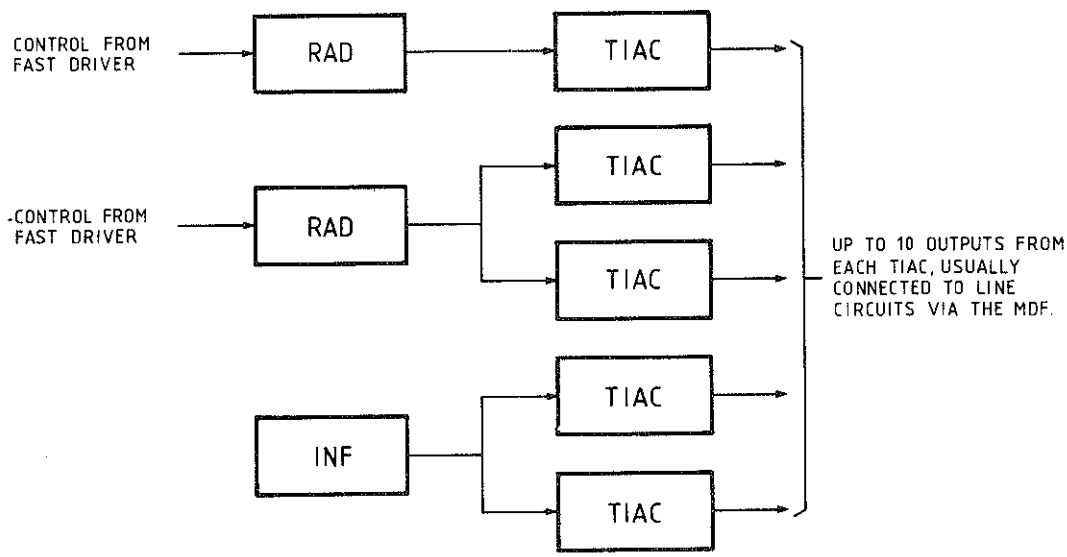

Figure 3.1. Principle of Tone Injection

The diagram shows a typical arrangement of the Tone Injection and Announcement Circuits (TIACs). The input to the TIACs are from tone generators or Recorded Announcement Devices (RADs) and these are selectable dependent on the requirements of the exchange. The RADs are started by a command from the Central Control Complex via a Fast Driver and normally last for a predetermined time interval. The tone generator shown in the diagram is for Information Tone (INF). Each TIAC can provide up to ten outputs for connection to the Switching Network. Therefore, if a service has to be provided to more points in the Switching Network (e.g. INF) the service must be connected to more than one TIAC.

3.1.8. Switching Network Control

All telephony lines have to be monitored so that any change in the condition of the lines will be detected and passed to the Central Control Complex for analysis. This is achieved by periodically scanning test points at the telephony units and at the LCs. This is carried out autonomously via a Tester and the status of the test points are passed to the Central Control Complex. Changes of the line conditions of

lines connected to a PMG, are signalled to the PCS via the Peripheral Channels. The CCC regularly polls the CCTs, to detect any event and, if one or more events are stored in a PCS, the information is transferred to the CCC.

The first change in line status is detected when the line changes from the idle state (e.g. a subscriber lifts his telephone handset and a closed loop condition is monitored at the corresponding Line Circuit test point).
In the case of an incoming line or a call on a high density local line, the IT or AJI respectively detect the status change.
For low density originating calls, the Central Control Complex, on receiving this status change, must search for a free AJ and connect the Line Circuit to this junctor. The software examines a record that it keeps of the condition of all the junctors connected to the same LB as the originating call. It also examines the condition of all the switches in that LB and when an unengaged, serviceable path to an unengaged, serviceable AJ is found, the Central Control Complex issues two commands. The first is to a Marker, to establish the path from the inlet of the LB to the free AJ, and the second is to a Slow Driver, to "Seize" the AJ. (The Marker and Slow Driver are part of the interface equipment).
The software ensures that seizing is spread equally over all AJ's available. if there are no available AJs or no free paths through the LB, the software places the call in a queue and periodically checks the condition of the exchange facilities until a connection to an AJ can be made. Telephony units which are to handle certain signalling methods such as keytones, multi-frequency codes, etc., are connected to Receiver units via the Trunk Link Network.
When the input is another public exchange or PABX, the IT or AJI, respectively, has to be connected via TB-A inlets and TB switches to TB-B inlets (B-side junctors). Once the software has found an unengaged serviceable path between the required TB inlets the Central Control Complex gives commands to establish the connection.

When the above paths have been established, the Central Control Complex gives a command, via the interface equipment, to connect the first dial tone to the line via the AJ, AJI or, if necessary via a Receiver. This will inform the subscriber that he may transmit the destination code.
The Tester will detect changes at the junctor or the Receiver when the subscriber transmits the destination code. This information is passed to the Central Control Complex and the software analyses the digits or group of pulses as they arrive and issues commands to remove the dial tone. If a second dial tone is required, commands are issued to connect this, via the AJ, AJI, IT or if necessary a Receiver, to the line to inform

the subscriber that he may continue dialling.

Once the incoming digits or pulses have been analysed and the destination of the call has been established, the Central Control Complex must investigate the status of the output lines and find a path through the TLN between the A- and B-side junctors.
The Central Control Complex examines whether the required output line is idle. When the output line is found to be engaged, busy tone (or its equivalent) is connected to the calling subscriber via the A-side junctor.
When the destination is a local low density traffic line and the line is not engaged, the Central Control Complex gives commands to connect the LC to an unengaged, serviceable B-side junctor circuit (BJ) and it gives commands to a Marker to switch through the path through the TLN, to establish the speech connection. The software distributes the traffic over all BJs, in a similar manner to that of the AJs.
When the destination is a P(A)BX line or trunk output, the BJO or OT has to be connected via a TB-B inlet to a TB-A inlet (A-side junctor). Once the software has found an unengaged serviceable path between the required TB inlets the Central Control Complex gives commands to establish the connection.

Once a connection through the exchange has been made, the A- and B-subscribers must be informed. When the B-side junctor is a BJ or BJO (i.e. a local terminating subscriber), the Central Control Complex gives a command via a Slow Driver to connect ringing tone and ringing current to the B-side junctor. The ringing tone is connected to the junctor in such a way that it is fed along the path to the A-subscriber and the ringing current is fed to the B-subscriber. When the telephone connection is via an OT to another exchange, the terminating exchange produces the ringing current for its own subscriber and passes ringing tone back along the telephone line for the A-subscriber.

The scanning mechanism detects a change at the B-side junctor when the B-subscriber lifts his handset.
The telephone call is now in the speech phase and the hardware removes the ringing tone and ringing current. The units are under constant surveillance during the speech phase but no action is taken unless the status of a changes (e.g. after reception of a metering pulse or reception of a release signal).
When either the A-subscriber or the B-subscriber replaces a handset, the status changes at the A-side or B-side junctor respectively. This information is detected by the subsystem and passed to the Central Control Complex. The software gives commands to release the relevant junctor, and via Markers, to release the relays in the TB-A, TB-B and LB (if the latter was used).

The only path that remains connected is from the other junctor to the other subscriber. (If the remaining junctor is an AJ, AJI, BJ, BJI or some types of IT, the software gives a command to connect busy tone (or its equivalent) to the junctor and hence to the remaining subscriber.
If the remaining junctor is an OT, a forward release signal is passed to the terminating exchange to initiate the release of the path.
In all cases, the remaining parts of the connection are released when the remaining subscriber replaces his handset or when the subscriber is placed in a forced release state.
The latter happens when the subscriber fails to replace his handset within a certain period of time and, once he is in a forced release state, he must replace the handset before another call can be made.

It is possible that, after a call initiation has been detected, a connection to the terminating subscriber cannot be made. This may be due to a lack of facilities in the exchange (e.g. there are no free paths, etc.,) or the terminating subscriber may be engaged. In all cases, the Central Control Complex gives commands to connect an appropriate tone (e.g. congestion tone, number unobtainable tone) to the A-side junctor.

3.2. Control Channel and Interface Equipment

All the peripheral equipments in the PRX/A system (Switching Network, utility equipment, etc.), are under the control of the Central Control Complex. The latter gives commands and inputs or outputs data via a Control Channel (CCH) connected to the Processor Terminal (PT) of Central Control Unit 0.

Most of the peripheral equipments however have a slow reaction time compared with the speed at which the Central Control Unit 0 can transfer information. Therefore, to reduce the time that the Central Control Unit 0 is involved with transfers to and from these slow equipments, interface equipment is provided. This equipment, shown in diagrams 107 and 108, consists of control channel terminals and various types of subsystems.

The subsystems may be fast subsystems such as Fast Drivers (FDs), Testers (TRs), Peripheral Control Subsystems (PCSs), Control Tape Reader and Punch (CTRP), Control teleprinter (CTEP), Data Link Subsystems (DLSs), or slow subsystems such as Slow Drivers (SDs) and Markers (MRs).

To improve the system reliability, the terminals and the control circuits of every subsystem are duplicated. The Central Control Complex governs which of the duplicated items is on-line and which is off-line and these conditions are periodically interchanged to allow duplicated items to be exercised equally. A pair of terminals together with a number of subsystems is called a Control Channel Subsystem Terminal Group (CSTG).

3.2.1. Control Channel Terminals

There are different types of terminal equipment for the CCHs. One type is the Control Channel Subsystem Terminal (CST), which is used for Fast and Slow Drivers, Markers and Testers. The other type is the Control Channel Terminal (CCT). The CCT is used to Control the PMGs via a PCS. Both terminal types have the same interface with the CCH. And both types can be used in a CSTG, the choice of the type depends on the type of subsystem. A CCT can be considered as a kind of CST.

3.2.1.1. Interfaces

Information transfers between the CSTGs and the main processors are executed via the allocated PTs and from each PT there is one CCH PT0.0 connected to all the CST0s (or CCT0s) via CCH0 and PT1.0 connected to all the CST1s (or CCT1s) via CCH1. Each CCH consists of up to three identical branches and up to ten CSTGs may be connected to each branch.
In addition to the CCH, two further control lines are connected to the CSTs from the PT. These are individual lines which allow the main processors to control the interface equipment configuration so that defective equipment may be isolated ("Data In" and "Data Out Connect").

3.2.1.2. Information Transfers between CCC and CSTs

A branch has an Outbus of 30 lines and an Inbus of 19 lines. (One line of the Inbus is provided for an autonomous request facility which at the present time is not used). A CST is capable of controlling nine subsystems.
Every transfer is initiated by the Central Control Unit 0 and consists of information passed to the subsystem followed by information accepted from the subsystem. When the Central Control Unit 0 requires a CSTG to carry out a function, it assem-

bles a 9-bit address word and a 20-bit data word and sends them via the Outbus to every CST. In addition, the Central Control Unit 0 generates a sync signal and sends this via the Outbus to initiate each CST. The CSTs in turn pass the 20-bit data word to their subsystems, the subsystems connected to one CST having a common data input highway and a common data output highway. Only the on-line CSTs decode the 9-bit address word and the CST that detects this address as belonging to one of its own subsystems (including itself) generates an individual Address Mark and sends it to the appropriate subsystem. The Address Mark is used by the subsystem to gate-in the data word, which includes the mode bits.

The subsystem returns a data word, (which may be the status condition of that subsystem or data from the peripherals) gated onto the common data output highway by the Address Mark and also sends an individual Confirmation signal to the CST. The CST checks the outputs of the subsystems, gates the data word onto the Inbus and generates a Sync signal. The latter is sent to the Central Control Unit 0, via the Inbus, to indicate that the data word is available.
If the CST detects an error in the above operation it will generate an interrupt to the Central Control Unit 0, which is able to test all subsystems and the CST by special commands.

3.2.1.3. Internal Subsystem of a CST

In addition to routing commands and data to and from the external subsystems, the CST has an addressable internal subsystem, capable of carrying out five principal functions.
The internal subsystem is capable of providing test data, or testing the CSTG error detecting circuits by simulating an error.
As previously mentioned, there are two CSTs per CSTG, each connected to separate control circuits in each external subsystem. One CST and its associated control circuits are online and the others are in the off-line condition.
To change the on-line hardware configuration a data word transfer is sent to the internal subsystems of both CSTs which, once decoded, resets a Preference flip-flop in the on-line CST and sets a Preference flip-flop in the off-line one. The Preference flip-flop in turn produces a Preference signal which enables the operation of the required CST and it is also sent to the associated control circuit of the subsystems to enable them.

Up to sixteen power supply testpoints are also connected to the internal subsystem and the status of these can be tranferred to the Central Control Unit 0 when requested.

3.2.1.4. Control Channel Terminal

The Control Channel Terminal (CCT) is an interface between a CCH and up to 7 subsystems such as the PCS. It may be regarded as a kind of CST and it has the same interface boundary with the CCH; the data transfer procedures, the method of addressing and the control of a preference condition, etc. are the same as for a CST.
The interface with a subsystem consists of a bi-directional parallel bus, called the Subsystem Control Channel (SCH). The CCHs and CCTs are duplicated equipment and the subsystem (PCs) can be accessed via one of two SCHs. Only one of these channels can be used, at a given time, depending on the preference condition of CCT0 and 1.
A data transfer between the CCC and CCT, in either direction, is initiated by the CCC when it executes an Input/Output instruction. The CCT is addressed and data is transferred to or from the CCT, depending on the instruction code. The CCT can send subsystem data, e.g. telephony events, or CCT-status data to the CCC.
When a subsystem, connected to a CCT, has data for the CCC, for example a telephony event, it sends an "attention signal" to the CCT and the "attention flag register" of the CCT is updated. This register is regularly read-out, by means of a special input (polling) instruction. If any of the attention flags has been set, the CCC will fetch the data, which is stored in a buffer of the subsystem(s), by means of a 'direct transfer' operation.

3.2.2. Marker

The Markers are used to operate the reed-relays whose contacts provide speech paths through the Link Blocks. The relays must be energised and de-energised by individual commands since once they are energised, they are self-holding (electrical latching method). To establish a connection through the LB or TB, three relays, one in each of the stages A..E or D..F must be energised.
This is achieved by routing an activating source to a selected access point in the LB/TB and providing a return path to each of the selected relays in the order C/F, B/E and A/D (i.e. a "vertical" is selected to "mark" the required relay). The return paths are common to a number of relays within one stage (they are connected to the same "vertical") so all the relays in that group are "marked". However, only one access point is chosen so only one relay per stage is energised. Only the provision of a release source at the required access point is needed to break-down the connection.

To provide the above sources to the Link Blocks, the Marker accepts data word transfers from the Central Control Unit 0 via the CST in the same way as other subsystems.
However, to identify the three return paths and the access point for the establishment of a connection, two data words have to be transferred. Only one data word is required to identify the access point when the connection is to be released.
The control circuits of the Marker decode the data words which identify relays in the Marker relay matrices. Once these relays are energised, their contacts provide activate or release sources and return paths for the Link Blocks.

3.2.3. Slow Driver

The Slow Driver is used to operate relays in the Switching Network, the contacts of which may be used to connect telephony units to the speech paths or to connect facilities such as busy tone, ringing current, etc., to these units. The relays must be energised or de-energised by individual commands since once they are energised, they are self-holding. To operate the required relay, the Slow Driver routes a positive (to energise) or a negative voltage (to de-energise) to one side of the relay.

The Slow Driver accepts a data word transfer in a similar manner to other subsystems. The control circuits decode the data word, part of which identifies a relay in the Slow Driver relay matrices. Once this relay is energised, its contacts provide the activate or release source to the required relay in the Switching Network.

3.2.4. Fast Driver

The Fast Driver is used for operations in the Switching Network under stringent real-time conditions. The Fast Driver accepts a data word transfer in a similar way to other subsystems. The control circuits decode the data word, part of which identifies a group of flip-flops in the Fast Driver matrix. Other bits of the data word provide the set or reset conditions for the chosen group of flip-flops. The outputs of the flip-flop matrix are used to control the Senders, Receivers, test units and some facilities of other telephony units. Since the FD flip-flops are staticised, the outputs remain active until the flip-flops are reset, dictated by real time conditions.

3.2.5. Tester

The tester is used to monitor the real-time status of test points in the Switching Network. The status of these test points will indicate the state of the peripheral equipment to the Central Control Unit 0 e.g. subscriber line not engaged, telephony unit seized, etc.. Two types of Tester are used in the PRX/A system, the Line Circuit Tester monitors the state of the Line Circuits and the Unit Tester monitors the state of the junctor circuits, Receivers and Senders.

The Tester contains a matrix of buffer circuits connected to, and holding the real-time status of, the test points.
The Tester accepts a data word transfer in a similar manner to other subsystems. The control circuits decode the data word, part of which identifies a group of buffer circuits in the matrix, and the status of these are gated out to the CST.

3.2.6. Peripheral Control Subsystem

The Peripheral Control Subsystem combines the functions of a Fast Driver and a Tester subsystem. The PCS is a later development in the PRX/A system.
The PCS does not control individual units, but it controls Peripheral Modules (PM) which may comprise a number of units. The Primary PCM Multiplexer, for example, is a Peripheral Module Group (PMG) which consists of two PMs and it contains a number of trunk circuits.
The data transfers between PCS and PM are "byte oriented". Each unit of a PM sends and receives information via the Peripheral Channel, which is the link between the PM and the PCS. A Peripheral Channel consists of multiplexed serial busses, operating with data frames of 32 bytes (8 bits). The maximum number of units in a PM is 32, each of which can send, and receive, one byte in a frame. In this way, one unit can send, and receive, one byte per multiframe (32 frames). The repetition time of a multiframe is 4 ms, so that the channel capacity for each PM is 64 kbit/s (for a "go" as well as "return" channel). These channels are used to receive the telephony events (such as a change of a line condition) and to send commands to the units.
A PCS can also send and receive one "housekeeping byte" per multiframe. This results in a capacity of 2 kbit/s for one housekeeping channel. There is one such channel for each PM.

The PCS has an independent scan function, which detects any change in the bytes received from each individual unit. When a change is detected, the event is stored in an Event Buffer of the PCS. The presence of one, or more, events is signalled to the CCT by activating the "attention signal", which is stored in the Polling Register of the CCT. A software controlled polling function of the CCC monitors the Polling Registers of all CCTs and if one or more "poll flags" are set, the events are fetched by sending IN instructions.
The PCS has a number of registers, which can be read or loaded by means of input/output instructions from the CCC. These registers are used for tests, error handling, housekeeping functions, etc.
The PCS is connected with the 2 CCTs via Subsystem Control Channels (SCH). The SCH is a bi-directional data bus. It comprises 16 data bits, the attention signal and a number of control signals.

3.2.7. Operators Position Control

The Control Teleprinter (CTEP) provides a means to control keyboard and printer of an operators position which can be a Teleprinter (TEP) or a Visual Display Unit (VDU) with a Hardcopy Printer (HCP). This position can be local or remote, the latter type controlled via a modem.
Data is passed between the main processor, the CTEP and a Utility Interface Box via the normal subsystem direct word transfer mechanism. The CTEP boundary is adapted to interface with the operators position boundary by the Utility Interface Box.
The control circuits on the CTEP decode the data word from the main processors, the mode bits indicating whether a keyboard or a printer operation is required. If a keyboard operation is required, the CTEP will gate the data held in a buffer to the CST, and if an output operation is required, the CTEP passes the relevant information from the data word received, to the printer or screen depending on the output device employed.
The CTEP also sends three interrupt signals directly to the Central Control Unit 0. The Keyboard Ready interrupt is sent to the processor to indicate that the CTEP has received information in serial form from the local or remote keyboard, has stored the information in parallel form in a buffer, and the CTEP is now ready to transfer the information.
The Printer Ready interrupt is sent to the processor to indicate that the CTEP has passed the required data to the local or remote printer and is available for a further data transfer. A Keyboard Error interrupt is used to indicate a fault.

The CTRP provides a means to control a cartridge system (up to three Cartridge Tape Units (CTU) possible) via the Utility Interface Box. The operation is similar to the CTEP in that the control of read and write operations depends on the mode bit received from the Central Control Unit 0.
The three direct interrupts used are a Read Ready interrupt, to indicate to the processor that the CTRP has received data from the cartridge system, the Write Ready interrupt to indicate to the processor that the CTRP has passed the required data to the cartridge system and is now available to receive further data from the Central Control Unit 0 and an Error Interrupt used to indicate a fault.
The operators' position can be used to select the tape-files, which have to be accessed. The cartridge systems can be used for storage of overlay programs, load tapes for dumping of subscribers' meter data, etc.. When an S-type memory is used a CTU can be used for the load/dump facility, which is to be used after an eventual system breakdown.

3.2.8. Data Link Subsystem

The Data Link Subsystem (DLS) is used to transfer data from the PRX/A to a remote station. This data can consist of Automatic Message Accounting (AMA) data, but also of other sorts of data. AMA data originates from calls which qualify for AMA. Data from various calls is stored in the Central Control Complex where it is arranged in blocks.

A DLS can control up to 6 data links and consists of a duplicated Data Link Control (DLC) and as many Data Link terminals (DLT) as there are links.
The Central Control Complex sends the data via the DLS, where it is assembled in complete blocks of 1024 bits, although incomplete blocks can also be sent. After sending a block the answers of the receiver are decoded and stored in the DLS, whereupon the Central Control Complex fetches the answers by means of a special command. If a block is received in a mutilated form, it can be repeated by the Central Control Complex.

The DLS can operate in full duplex and in half duplex mode; in the latter case the transmit and receive modes can be selected. The options mentioned above can be selected by means of straps and do not affect the software. The selection depends on the properties of the receiver.

3.3. Central Control Complex

The Central Control Complex (CCC), shown in DB-A 7400e/3-104 consists in maximum configuration of the following parts:

- Central Control Unit 0 (CCU0) (main);
- Central Control Units 1 and 2 (CCU1 and CCU2) (secondary);
- Memory Switch 0 and 1 (MS0 and 1);
- Central Memory 0 and 1 (CME0 and 1);
- Master Subsystem Distributor 0 and 1 (MSD0 and 1);
- Configuration Control Switch 0 and 1 (CCS0 and 1);
- Test Access Circuit Switch (TCS);
- Master Switch Unit (MSU).

Each Central Control Unit consists of two processors (PRs) and two Processor Terminals (PTs). Processor and Processor Terminal are basically similar for all control units. Differences due to the main and secondary tasks of the control units are described in the processor and Processor Terminal description below. The Central Control Complex in minimum configuration, consisting of one Central Control Unit only, shown in DB-A 7400e/3-103. The Test Access Circuit Switch, Master Subsystem Distributor and Configuration Control Switch are not necessary.
The Master Subsystem Distributor and Configuration Control Switch have to be installed when the system is extended with a Memory Switch. The Test Access Circuit Switch has to be installed when the system is extended with a Central Control Unit (secondary), to provide test paths from the main processors to secondaries.

3.3.1. Processor
(see DB-A 7400e/3-110,111)

The processor consists of the following parts:

- Input/Output Unit (IOU);
- Processor Control Unit (PCU);
- Arithmetic Unit (AU);
- Central Processor Unit (CPU);
- Processor Memory (PME);
- Standard Boundary Adapter (SBA);
- Alarm and Switching Unit (ASU);
- Test Access Circuit (TAC);
- Processor Control Panel (PCP).

3.3.1.1. Input/Output Unit

The IOU controls all input and output of data to and from the Control Channel, the ASU and the MSD (for main processor only). The initial control for each function is governed by the CPU but the IOU can complete some functions independently, enabling the CPU to carry out other tasks.

The IOU is involved in the following operations: direct transfers, autonomous transfers, autonomous scanning and interrupt routines.

3.3.1.1.1. Direct Transfers

The conveyance of single data words to and from subsystems over the CCH are possible by direct transfers, initiated by a program instruction from the CPU. Part of the instruction gives the address of the subsystem and this is put in the IOU Address Register. Decoding of other bits of the instruction causes a data word from the AU to be put in the Input/Output Data Register together with two mode bits (IN and F bits). The destination address and the output data are passed to the Outbuses and the IOU control generates a Sync signal which is also passed to the Outbuses to indicate that the information is available on the CCH. Once the addressed subsystem group has accepted the information the CST responds by putting a data word on the CCH and generating a Sync signal. The data is passed by the Inbus to the Input/Output Data Register and the IOU control will transfer this data to the AU when it receives the Sync signal.

The CPU can transfer data to and from the IOU, TAC and ASU by addressing these units as it does other subsystems. However, for direct transfers to these internal units, no Sync signal is generated.

3.3.1.1.2. Autonomous Transfers

Some subsystems have an autonomous transfer facility which enables the processor to transfer a block of data, one word at a time either to or from that subsystem without disturbing the contents of the program accessible registers.

The autonomous transfer request has priority over instructions, interrupts and autonomous scanning, all of which are suspended when the autonomous transfer takes place. The processor Terminal passes the autonomous transfer request generated by the subsystem via the IOU to the Main Sequencer in the

CPU.

Once the request is accepted, the subsystem address from the PT is modified, put in the IOU Address Gates and also sent to the CPU where it is used to access the required autonomous transfer control locations of the memory. A reset signal is sent from the IOU control to reset the staticizers in the PT. The control locations in the memory are read and the mode bit is transferred to the Input/Output Data Register. If the mode bit indicates a write operation (IN = 1) the data and F bits of the Input/Output Data Register are zero. If the mode bit indicates a read operation (IN = 0) the data is read from the data buffer in the memory and transferred with the mode bit to the Input/Output Data Register. In both cases the IOU generates a Sync signal and the information in the Input/ Output Data Register together with the Sync signal and the subsystem address in the Address Register are passed to the PT as a direct transfer. If the autonomous transfer is a read operation the CPU resumes its original task as soon as it has passed the outgoing data to the IOU. The IOU remains busy until it receives the incoming Sync signal.
If the autonomous transfer is a write operation, the IOU on reception of the Sync signal transfers the incoming data from the PT to the CPU via the Input/Output Data Register.
The CPU resumes its original task as soon as it has written the data into the memory.

There are two control locations in the memory for each subsystem that has the autonomous transfer facility. These locations, apart from indicating the mode of operation also contain a count of the data words (block lenght) to be transferred and the address where the outgoing data is stored or where the incoming data is to be put in the memory.

3.3.1.1.3. Autonomous Scanning

Autonomous scanning is a feature of the IOU to save processor time. By means of the autonomous scanning mechanism the IOU can monitor the test points of telephony units and Line Circuits, via a Tester subsystem, in order to keep the software informed about the traffic situation. Autonomous scanning is performed only in Central Control Unit 0 because only this control interfaces with the Switching Network.

Before the software issues a "Start Scan Series" to the IOU it has prepared scan data structures, so called Scan Control Packets. In each packet information is present for the IOU to scan up to 15 scan blocks. The number of scan strokes (up to 64) which have to be executed is indicated in each block.

A scan stroke results in 16 data bits, each representing one test point of a Tester Horizontal. In this way one block corresponds with the 64 possible horizontals of one tester. Autonomous scanning consists of a number of scan strokes each stroke being one output/input transfer identical to a direct transfer. During a scan stroke, controlled by the IOU, the Central Control Unit 0 can carry out other tasks.

Once the software has prepared scan data structures (see 4.3.1.2.1.) the CPU issues a "Start Scan Series" command to the IOU.
Provided the IOU is not busy, it responds with a "Scanner Start Data Request (SSD). The address of the subsystem (Tester), the number of scan strokes, the address of the old scan result table in the memory are transferred to the IOU from the prepared data structure (Scan Control Packet).

The "Next Scan" signal is given which makes the IOU busy and initiates one scan stroke which is a direct transfer carried out by the IOU i.e. the output data (tester horizontal to be scanned) is transferred together with a Sync signal and subsystem address, to the CST via the CPT.

The Sync signal returned by the CST loads the Input/Output Data Register with the new scan data from a Tester Horizontal and a "Compare" request is generated. In this operation the address of the old scan result is passed on to the CPU and old scan result is sent to the IOU where it is compared with the new state received from the Tester.
If a difference is detected between the old and the new results, three autonomous transfers are requested in succession to produce a "Result Buffer". These autonomous transfers have priority over externally generated autonomous transfer requests but otherwise they are processed in the same way.
The three data words transferred to the "Results Buffer" are the old state address, the new state value and the logical difference between the new and the old states.

At the end of the three autonomous transfers or during the "Compare" routine, if no difference is detected the IOU checks the progress of the autonomous scanning. Another IOU scan stroke is carried out if the current Scan Block has not been completed.
Otherwise a SSD request or "End of Scan" interrupt is generated if a new scan block is to be processed or if all the scan blocks have been completed respectively.

3.3.1.1.4. Polling

The autonomous scan function is only used for collecting events from units which are monitored by a Tester. Units controlled by a PCS are "scanned" in two separate stages. The PCS receives the bytes from each unit in an Input Register and autonomously compares the new bytes with the corresponding old ones, which are stored in a memory of the PCS. An event is constituted, when a difference is detected, and stored in the Event Memory. The presence of one or more events is signalled to the CCC by setting a "polling flag" in the CCT.
The "second stage" is controlled by the software of the CCC. The polling flags of all CCTs are monitored periodically. When one or more flags are set, input instructions are issued, to fetch the associated events. The Poll Register of a CCT contains 7 bits, the number of which corresponds with the number of subsystems that may be connected to a CCT. When the flag of one of these subsystems has been set, the Event Memory of that subsystem is read-out, until the Event Memory has been emptied, or until a maximum number of events are fetched.
In the latter case, the polling flag is not reset, so that the remaining events can be fetched in the next cycle. In this way the event handling of a PCS can not be delayed indifinitely, due to abnormal high event rates of another, preceding PCS.

3.3.1.1.5. Interrupt Routine

The IOU holds an interrupt mask which is passed to the PT and used to inhibit all interrupt requests on or below the current program priority level. When an interrupt request occurs above this priority level a general request signal is passed to the IOU control and the relative interrupt group address is passed to the IOU Address Gates. The main IOU receives requests from both PTs (i.e. those of PT0 and PT1) and passes the one with the highest priority to the CPU. (If both are of the same priority, the request from PT0 is accepted first).

The CPU saves the current contents of its registers and initiates a program to deal with the interrupt. The CPU also sends an Interrupt Response to the PT to reset the Inbus control and prevent a change to the selected interrupt group. The IOU sends a "Load Interrupt Status" signal to the PT which causes the interrupt group information to be passed via the Inbus to the IOU together with a Sync signal.
The Sync signal allows the interrupt group status to be loaded into the Input/Output Data Register and passed to the CPU. The program initiated by the interrupt will pass a new interrupt

mask to the IOU before processing the new interrupt.

3.3.1.2. Processor Control Unit

The PCU co-ordinates all the operations of the processor. It interprets and obeys program instructions regulates the main sequences and directs the flow of data.
For the majority of the time, the processor is operating under the control of the software (i.e. the PCU is obeying program instructions taken from the memory). However, on request, the Main Sequencer circuit of the PCU can intervene in this operational process after each program instruction to allow the hardware to carry out a "Main Operation". These operations in their order of priority are:

1. Halt;
2. Dual Error Interrupt Routine;
3. Trace Interrupt Routine;
4. Autonomous Transfer (called by the scanning process);
5. Autonomous Transfer (external);
6. Recovery Alarm Interrupt Routine;
7. Interrupts;
8. Scanner Start Data Request;
9. Compare Request.

Further details of operations 1,2,3 and 6 are given in chapter 7. Operations 4,5,7,8 and 9 have already been described. The programs are run with the aid of the Instruction Register, Address Selection Register and the Program Counter. The Instruction Register is loaded with each instruction word read from the memory. The word is decoded and the output distributed throughout the processor. The Instruction Register may also be loaded with a pseudo instruction code for the other "Main Operations", although these codes are not permitted in program instructions. The Address Selection Register holds the address of the next memory location to be read. This address may be either the address of the next program instruction, an operand address or the address of any location in the memory needed to be accessed during an operation. The Program Counter contains the memory address of the next program instruction.

The PRX/A processor is a consecutive operation machine and the content of the Program Counter is advanced by one by the AU after each instruction access. The content of the Program Counter is changed during a jump instruction, program interrupt and restore operations.

A program instruction consists of a number of microprograms, each one identifying a particular hardware routine. There are

special microprograms applicable to individual instructions (e.g. shift left register A) and common microprograms applicable to many instructions (e.g. jump).
The latter are sometimes carried out in parallel with other microprogram. (e.g. OK cycle). A microprogram consists of one or more cycles, each cycle carrying out a detailed part of the hardware routine. There are two types of cycles, an A cycle for reading the contents of a memory location and a B cycle for writing to the memory and/or executing part of an instruction. Both types consist of eight time pulses, derived from their own Clock Pulse Distibutor and both distributors Clock Pulse Generator).
The microprogram being executed at any instant is dependent on the program instruction decoded and the condition of phase flip-flop. As program instructions have more than one A and/or B cycle, the phase flip-flops are used to identify which cycle is in progress.

The Master Clock Pulse Generator is in the PCU and under the control of the Main Sequencer. One of the timing signals also produced initiates the memory read cycle which in turn gives a "Read Ready" signal after the cycle is complete.
The Master Clock Pulse Generator receives this "Read Ready" signal from both PCUs to ensure that both processors are synchronised in the dual mode.

3.3.1.3. Arithmetic Unit

The primary function of the AU is to perform arithmetic and logic operations under the direction of the PCU.
The execution of instructions and other hardware operations requires a sequence of arithmetic operations such as the incrementation of the Program Counter contents, the computation of the operand address, transfer of data from one register to another, etc.. The AU is also employed for input and output data transfers via the IOU.
Data lines are provided to link the AUs of both processors of a pair. In the dual mode of operation, each AU passes the contents of the memory register to the other AU every A and B cycle. Each AU compares the contents of its own register with that of the other processor. The memory register acts as a buffer for data transfers in both directions between the AU and the memory. Therefore the majority of hardware errors in each Central Control Unit will affect the contents of the register of only one processor and the comparison carried out by both AUs of that pair will detect these errors.
The data lines are also used by an on-line processor wishing to update the off-line one in preparation for the dual mode of operation.

3.3.1.4. Processor Memory

The Processor Memory in the PRX/A system can contain up to eight Memory Modules, each module having a capacity of 32768 eighteen-bit words (including a parity bit and a protection bit). For the purpose of the software organisation the modules are divided into four banks. The CPU addresses all the banks simultaneously and presents the data word to all the modules in parallel.
The commands to read or write however, are only sent to one module dependent upon a PCU command and so only one location in the memory is activated. The memory is used to store program instructions, permanent data and temporary data.

3.3.1.5. Standard Boundary Adapter

In addition to the processor memory each processor can access a Central Memory (if installed) via the Standard Boundary Adapter (SBA) and a Memory Switch (if present).
The Standard Boundary Adapter can be directly connected to a Central Memory, when this is used as an extension memory smaller than or equal to 256K.
The selective read or write PCU command causes the SBA to issue an allotment request to the Memory Switch or to Central Memory (if directly connected).
In the latter case, and also when only one Central Control Unit is present, this allotment request is immediately answered with a processor allotment. When there are more Central Control Units a priority decoder in the Memory Switch decides which processor is allotted when more than one Central Control Unit requested an allotment at the same time. (Priority: 1:CCU0; 2:CCU1, 3:CCU2 4:DMA).
After allotment of the processor the Memory Switch is a completely transparant device. Standard Boundary Adapter and Central Memory follow a hand-shake procedure to transfer data to and from the Central Memory (see 3.3.4.). When data-transfer is completed SBA sends a Release Request and the Memory Switch terminates the processor allotment.

3.3.1.6. Alarm and Switching Unit

The ASU carries out three main functions. The ASU contains a 2,1191 MHz Xtal oscillator which drives divider circuits to produce a Real Time Clock (RTC) interval of 12,5 ms. The RTC is initiated by a command from the CPU.
When the RTC reaches it's final value, it resets itself and generates a RTC interrupt which is handled as a normal inter-

rupt by the PT. The clock remains in its reset state until the software accepts the RTC interrupt, generates a new start command and passes the command via a direct transfer to the ASU. If the clock remains in the reset state for longer than 500 seconds (due to an error), an OK interrupt is generated and passed via the PT to inform the software.

Continuity of a processor is maintained when the continuity relay in the ASU is energised. Under normal operating conditions, this relay is kept energised by correct functioning of the RTC loop. This loop involves a large amount of hardware RTC, PT and a large amount of CPU circuitry) and the software used for answering an RTC interrupt. Consequently if a new RTC start command occurs within the correct time interval, it implies that the software considers the state of the hardware correct and the continuity relay is kept energised. When a hardware or software error causes discontinuity, the ASU initiates alarming and configuration switching (to protect the system against faulty outputs).
A main processor can stop a secondary processor by opening the RTC loop. A main processor command to the Configuration Control Switch de-energises a relay and a contact of the relay opens the RTC loop.
When both main processors have lost continuity (double discontinuity) due to an error, the Master Switch Unit sends recovery interrupts to the ASUs of both processors alternately.
When both processors of Central Control Unit 1 or 2 have become discontinuous Central Control Unit 0 can send recovery interrupts via the Configuration Control Switch to the AU's in order to start the processors.
The CPU can access the ASU by means of a direct transfer. The data word transferred from the IOU to the ASU may be either a control command or a status request. The ASU can obey a number of commands to perform alarm and switching functions related to the processor and its CCH boundary, DCH boundary, memory boundary and the boundary with the other processor. The ASU also keeps a record of the Memory status, Boundary status, Configuration status, Command status and Error status.

In the latter case, any error occurring in the processor (i.e. Parity Error, instruction time out, etc.) will be staticized in the ASU, the ASU will generate a Processor Error Interrupt and this will be passed to the PT of both processors. The software, on accepting the interrupt must initiate a direct transfer to receive the error status. Via a direct transfer, the software may give test commands to check various circuitry.
The Central Control Unit 0 can initiate a Dual Error Interrupt (see 3.3.1.2.) in the ASU of a Central Control Unit 1 and 2 via the Configuration Control Switch in order to start an error program.

A dual error alarm generated in the ASU of a Central Control Unit 1 or 2 is fed to Central Control Unit 0 in order to make this control unit (and the other Central Control Unit 1 or 2). also start an error program, because the error could have been in all processors e.g. a miscompare in data from the central memory could have been initiated by a fault in another processor. Main and secondary processors can communicate to exchange e.g. testresults after an error program by means of two communication bits fed from the main processors IOU via Master Subsystem Distributor and Configuration Control Switch to the ASU's of the secondary control units (forwards and backwards).

3.3.1.7. Test Access Circuits

The PRX/A system has the facility to use a main processor to test the other main processor or the secondary processors. Diagnostic programs in an off-line main or secondary processor may be controlled from the on-line main processor via the TAC of the off-line processor.
The TAC decodes the commands received from the on-line processor and initiates actions in its own processor. These actions may result in returning information to the on-line processor for further processing or passing information to either the Technical Display Panel or Processor Control Panel for display.
Two types of TAC path are possible namely a path from the on-line main processor via the Master Subsystem Distributor to the TAC of the off-line main processor and a path from on-line main processor to off-line secondary processor via the Master Subsystem Distributor and Test Access Circuit Switch. Before using the latter path the main processor has to send an Enable TAC signal to the Test Access Circuit Switch and the off-line processors TAC via the Configuration Control Switch. When a path is established, it can be seen as completely transparent. A main processor TAC is enabled when it receives the discontinuity signal from its own ASU and the continuity signal from the other ASU. A secondary processor TAC is enabled when it has received the Enable TAC signal.
The IOU of an on-line main processor controls the operation of the off-line processor by generating a direct transfer addressed to the off-line TAC. The data word passed in this transfer is a command for the TAC to obey. It is accompanied by a Sync signal and when required the "IN" mode bit and clock signal. The TAC, being an internal subsystem (like the IOU and ASU) does not return a Sync, signal and if a data word is expected from it, the on-line IOU will gate the word via the Input/Output Data Register to the AU by internal control.

3.3.1.8. Processor Control Panel (see diagram 116)

Each processor is equipped with a PCP to provide a complete status of the processor. Each panel is under the control of a key and pushbutton on the System Control Panel (see paragraph 3.4.) and may also be used to initiate or block operations of the processor during off line testing and abnormal situations.

3.3.2. Processor Terminal

The Processor Terminal consists of a Control Channel Processor Terminal (CPT), an Autonomous Transfer Allotter (ATA), an Interrupt Allotter (IAL) and a Subsystem Switching Unit (SSU). Processor Terminals belonging to main processors (CCU0) and those belonging to secondary processors (CCU1, CCU2) are simular. However due to the fact that secondary Processor Terminals are not interfacing with the Switching Network, CCH functions related to that interfacing task are not used.

3.3.2.1. Control Channel Processor Terminal

The Control Channel Subsystem Terminals are connected to the Control Channel Processor Terminals of Central Control Unit 0 only. Data signals are transferred into and out of the CPT via line/logic converters at the Inbus and Outbus respectively. Data for transfer from the Processor to the CSTs is passed to the Outbus together with an address and a Sync signal.
The data is from the Input/Output Data Register, the address is from the IOU Address Register and the Sync signal is from the IOU control. The response from the CST or subsystem is checked for parity and passed to the Input/Output Data Register in the processor. The incoming Sync signal is passed to the IOU control and the CST interrupt if one occurs is passed from the Inbus to the Interrupt Allotter. In all Central Control Units data transfer from CPT to SSU and from IAL to CPT takes place, these are described in 3.3.2.3. and 3.3.2.4.

3.3.2.2. Autonomous Transfer Allotter

An optional facility can be provided so that up to a maximum of seven subsystems are able to communicate with the processor by an autonomous transfer method.
The Autonomous Transfer Allotter staticizes the requests (from the subsystems that wishes to use this communication method) as a group and presents them one at a time according to their priority, to the IOU together with their address.
During this process if further autonomous transfer requests arrive, they are collected as another group and will not be processed until the lowest priority request of the previous group has been completed.

3.3.2.3. Interrupt Allotter

The Interrupt Allotter controls the order in which the majority of the program interrupts are offered to the processor. A few program interrupts are connected directly to the processor Main Sequencer. The IAL has eight priority interrupt groups each of which can contain up to sixteen requests giving a maximum total of 128 possible program interrupts. The processor provides an interrupt mask to the IAL to indicate which priority groups may not interrupt the current program.
When an interrupt signal in an unmasked level arrives at the PT the IAL sends a request via the IOU to the Main Sequencer and sends the priority group address to the IOU Address Gates. The processor, on accepting the request, calls for the interrupting level status. This sixteen bit word in the IAL is gated onto the Inbus (CPT) and transferred to the processor.

A selective reset signal deletes these requests from the priority level request buffers in the IAL. The processor blocks itself to further interrupts until it has adjusted the interrupt mask in accordance with the new program level. The highest priority group is designated for the processor error interrupts and this group is never blocked by the interrupt mask.

3.3.2.4. Subsystem Switching Unit

The SSU of a main processor (CCU0) is used to isolate defective CSTs and subsystems so as to protect the operating part of the system from the influence of the defective equipment. The SSU receives direct transfers from the IOU via the Outbus in the same way that data is transferred to the interface equipment. The SSU responds with a Sync signal to the In-

flip-flops may be set or reset in the SSU and the flip-flops energise relays and provide logic level outputs.
The relays are situated in the CSTs (two in each CST) and are used to inhibit the data from the CST to the PT and/or the data from the subsystems to the Switching Network. The logic level outputs are used to test the interrupt mechanism (i.e. they set request flip-flops in the IAL). The latter feature is also used in all secondary processors.

If a defect should occur in the SSU, which prevents the software controlling the flip-flops, they can be reset by the Alarm and Switching Unit in the processor.

3.3.3. Memory Switch

The Memory Switch makes a datapath available between one out of four possible members and one out of three Central Memory parts after an allotment procedure between a member and the Memory Switch. The allotment procedure and the datatransfer between a member and the Central Memory are asynchronous and follow a handshake procedure. The four possible members are the main processor, the two secondary processors and a Direct Memory Access (DMA). If more than one member does an allotment request at the same time first the member with the highest priority is allotted. (priority: first CCU.0 then CCU.1 then CCU.2 and then DMA). When that member is finished the next lower priority member can make a data-transfer.
Between Memory Switch 0 and Memory Switch 1 synchronisation signals ensure synchronism in dual operation.
Correct operation of the Memory Switch can be tested by test commands from the CCS, which also controls Memory Switch-Central Control Units configuration and receives MS status information.

3.3.4. Central Memory

When only one processor pair (main) is present the Central Memory in fact is an extension memory, which can operate with or without a Memory Switch. A Memory Switch is not necessary for extension memory of up to 256K capacity. When memory capacity is greater than 256K it is advisable to use a Memory Switch to increase reliability due to the possibility of configuration switching.
A central or extension memory can consist of up to three modules, each of 256K words of 18 bits. The memory can be of a semi-conductor type or core type (Q14-H2). For the latter, a Q14 Adaption Box (QAD) is present to convert Q14 signalling

procedures into standard boundary procedures.
These procedures are asynchronous and of a handshake type. Two types of procedures can be distinguished: a command transfer and a result transfer.
The processor starts a command transfer by sending a Sync for Command Transfer, which gates the corresponding address-, data- and control- bits into the Central Memory. After correct reception the Central Memory replies with Acknowledge for Command Transfer. The processor now withdraws the Sync for Command Transfer whereupon the memory withdraws the Acknowledge for Command Transfer. The data path is still maintained in the Memory Switch because the command transfer is always followed by a result transfer to send the required data back to the processor.

The memory starts a Result Transfer by sending one of two possible Sync's for Result Transfer (SRT0 or 1), SRT0 when the preceding command was a read command and SRT1 when it was a write command. The handshake procedure is then identical as described above. The processor replies with Acknowledge for Result transfer, which is followed by a withdrawal of Sync for Result Transfer 0 or 1 and Acknowledge for Result Transfer in succession.

3.3.5. Master Subsystem Distributor (see diagram 112)

The Master Subsystem Distributor (MSD) has the task of decoding the correct address from the commands originating from the main processor IOU and distributing the data to various destinations.
These destinations are:

- Configuration Control Switch (own and other side);
- TAC other main processor;
- TAC Switch (TCS) (secondary processor TAC's).

The mode bit IN, sent from the IOU to the MSD, controls the direction of the transfer.
Commands to the Configuration Control Switch are always sent in two words. The first word giving the address of the CCS and the address of the CCS output, is buffered in the MSD until the second word with the real command arrives and then both types of information are sent to the CCS together.

3.3.6. Test Access Circuit Switch

The TAC Switch distributes commands and data received from the IOU of the main processor (on-line) via the MSD to the TACs of the secondary processors (off-line). The TCS can receive data from MSD0 or 1, preferency of an MSD being controlled by Configuration Control Switch 0 or 1. Data, which is fed to all secondary processor TAC's in parallel is selectively gated into a TAC by an Enable TAC command from the CCS. The same command also selects a backward datapath in the TCS, from where the backward data is fed via both Master Subsystem Distributors to the main processors.

3.3.7. Configuration Control Switch

As is shown in diagram 104, two Configuration Control Switches are present; CCS0 controlling the "0" part of the Central Control Complex and CCS1 the "1" part.
Each CCS can receive data, control and address signals from the Master Subsystem Distributor 0 and 1 (see diagram 112).
As long as the own side main processor stays continuous the own side MSD is preferent. An automatic change over to the other side MSD occurs when the own side main processor becomes discontinuous.
The address bits from MSD to CCS select the destination in the CCS. Each CCS has the following destinations on the own side (see diagram 113):

- Main processor 0,;
- Secondary processors 1 and 2;
- Memory Switch;
- Test Access Circuit Switch.

A command register exists in the CCS for each of the destinations above. Configuration signals from the main processors ASU enable the CCS to offer the contents of the command register to the destinations. When a main processor is off-line it is possible to enable both CCS0 and CCS1 outputs from the other still continuous main processor. In this way a cross configuration can be set up.
The MSU sends recovery signals alternately to a main processor, via the CCS (when present, otherwise directly), when both main processors are discontinuous. The continuity signals from the main processor are also fed via CCS0 and CCS1 to the MSU.
An ASU of the main processor can receive two types of error signals from the CCS, a Dual Error Interrupt and a Single Bit Error.
A dual Error signal is derived in the CCS from status signals

from secondary processor and Memory Switch and is fed to the main processor ASU to initiate a Dual Error Interrupt. The main processor also starts a Dual Error program in the secondary processors, because a Dual Error can have been caused by any processor via the Central Memory.
A Single Bit Error is generated in the Central Memory (semiconductor only) when one bit of a word read out of memory was wrong and has been corrected. A Single Bit Error starts an interrupt via the Interrupt Allotter.
Via the CCS, a main processor is capable of starting and stopping a secondary processor and initiating Dual Error Interrupt. A recovery signal starts a main processor and by means of withdrawing the allow continuity signal a secondary processor can be forced off-line.
By means of two communication bits a main processor can communicate to a secondary processor via the CCS in order to exchange test result information.

Configuration commands are present in the CCS to control the Memory Switch standard boundary configuration and for selection of the required TAC paths.

Test commands for the Memory Switch are used to test the Memory Switch allotting mechanism.

3.3.8. Master Switch Unit

The MSU receives, under normal operating conditions, a continuity signal from both main processors ASU's of CCU0 (via the CCS if present).
The MSU takes no action if one of the continuity signals is absent. However, if both signals are absent, the MSU sends a "Start Recovery" signal to each ASU alternatively until one main processor is able to respond with a continuity signal again.

3.3.9. Technical Display Panel (see diagram 117)

The Technical Display Panel (TDP) can be connected with each processor to provide diagnostic facilities. The panel has some control buttons and a number of lamps to indicate the contents of all the important processor registers and control flip-flops. Data is passed to the TDP via the TAC.

3.4. Utility Equipment

The utility equipment is a group of special equipment which permits man/machine communication, for operational and maintenance purposes, and the testing of the Switching Network.
This group comprises an operators position (Teleprinter or Visual Display Unit with Hard Copy Printer), up to 3 Cartridge Tape Units (CTU), a System Control Panel (SCP), a Transportable Testpanel (TTPA) and integrated test equipment.
The operators position and CTUs are connected to the CTEP/CTRP via the Utility Interface Box (UIB). It is also possible to connect a remote operators position. This remote position can be connected via modems. When a Management and Maintenance Centre (MMC) is used, this is connected via a data link which terminates, at the exchange side, on a Utility Processor (UP), which is connected to the UIB. The UP also controls the (serial) data flows between the PRX/A and local operators position, so that no interference can occur between the local operators position and the one in the MMC.

3.4.1. Operators Position

The operators position provides the main means of man/machine communication in the PRX/A system. A built-in modem in the exchange (optional equipment) makes it possible to connect a remote operators position which has the same facilities as the local one. The selection, remote or local, is done at the Utility Interface Box. The system is normally controlled from the remote positions, installed in a management centre.
The operators position is a low speed device and its function is to report primary system events (e.g. alarms), logging and transferring to the Central Control Complex operational transactions and reporting secondary system events. The system prints messages autonomously. When these messages involve alarm reports, they can interrupt any other operational positions event. The operator in his turn can interrupt the reporting of secondary events.

3.4.2. Cartridge Tape Unit

As an alternative to the operators position, the input or output of information may be accomplished via the Cartridge Tape Unit. Reading and writing speeds are much higher that those of the TEP or VDU. Consequently it is preferable to use this device when large quantities of operational requests or extensive system reports have to be handled. When a semi-con-

ductor type memory is used, one or more cartridge units may be reserved for autonomous dumps of semi-permanent data and as a back-up store for permanent data.
Up to three Cartridge Tape Units can be connected to the Utility Interface Box, which controls the Cartridge Tape Units. Each unit contains two Cartridge Tape Drives (CTDs), each cartridge contains four tracks with storage capacity of 635 kbyte/track, giving a total capacity of 5 Mbyte per Cartridge Tape Unit.

3.4.3. System Control Panel (see diagram 114)

The main purpose of the SCP is to provide a quick survey of the system condition. On this panel, various kinds of information of interest to the maintenance personnel are displayed and a limited number of manual control facilities are provided. Alarm conditions are indicated by lamps on the SCP and also in some cases by audible means. Buttons are provided to control these alarms. Lamps are also provided to show the service condition of equipment. When one or more devices of an equipment type is "out-of-service" or "in-error" the appropriate lamp indicates this. Further lamps are provided to display the CCH current configuration. The manual facilities on the SCP enable load procedures or tests to be executed.

3.4.4. Transportable Test Panel (see diagram 115)

The Transportable Test Panel provides a means for manual and visual communication with the Central Control Complex to enable the manual control of hardware tests on controlled equipment. From the TTPA, the Central Control Complex can be instructed to set up test conditions in readiness for a hardware test, after which the results are displayed step by step. All hardware except the processors can be tested in this manner. Interface equipment is tested by simply specifying command data to be sent and inspecting the response data. For testing Switching Network equipment all operational conditions can be simulated by special integrated (or external) test equipment under program control. A listening-in facility is also present on the TTPA.

3.4.5. Integrated Test Equipment

The system is equipped with integrated test equipment which is under control of the CCC, interfaced by Testers and

Fast Drivers. The purpose of most of this test equipment is to generate signals and check the responses to these (go/no go tests) to establish whether the equipment under test is functioning correctly. Other test devices detect audio signals, match the handset of the TTPA to the network, etc.. The test equipment can access the telephony network via appointed inlets on the TB's and LB's. The test equipment is connected to a matrix (Network Access Matrix), which can interconnect it under program control to the test inlets. The matrix can form more than one path at a time, if the test requires it. The test of a telephony device is a simulation of all normal conditions the device can meet. Therefore the device is given commands via its drive points, by the normal telephony handling programs. Under control of test equipment handling programs, the test equipment generally simulates the calling party in a normal call. The programs derive their input information from simple button manipulations on the TTPA which also displays the state of the test object and connection in telephony oriented terms. The button manipulations may also be replaced by testprogram instructions input via the keyboard or tape.
The system can be instructed to send tone commands to a unit under test (e.g. busy tone, congestion tone or second dial tone). It is therefore possible to test tone sending functions without having to simulate traffic conditions.

Various external test equipment can be connected to the PRX/A system to suit individual needs. For example, the system can be equipped with a called-party simulator which, when called, automatically simulates all actions of a normal subscriber.
The called-party simulator is connected to a Line Circuit as a normal subscriber. It can be selected by its directory number or by an abbreviated code. Subscribers lines can be tested in a number of ways. These tests can be executed as routine tests and as manually controlled tests. A VDU is used to initiate the scheduling or to control the tests. If the exchange is connected to a remote maintenance centre, the tests can be executed from that centre. It is also possible to get access to the live measuring equipment from the subscribers premises, by dialling pre-determined numbers.

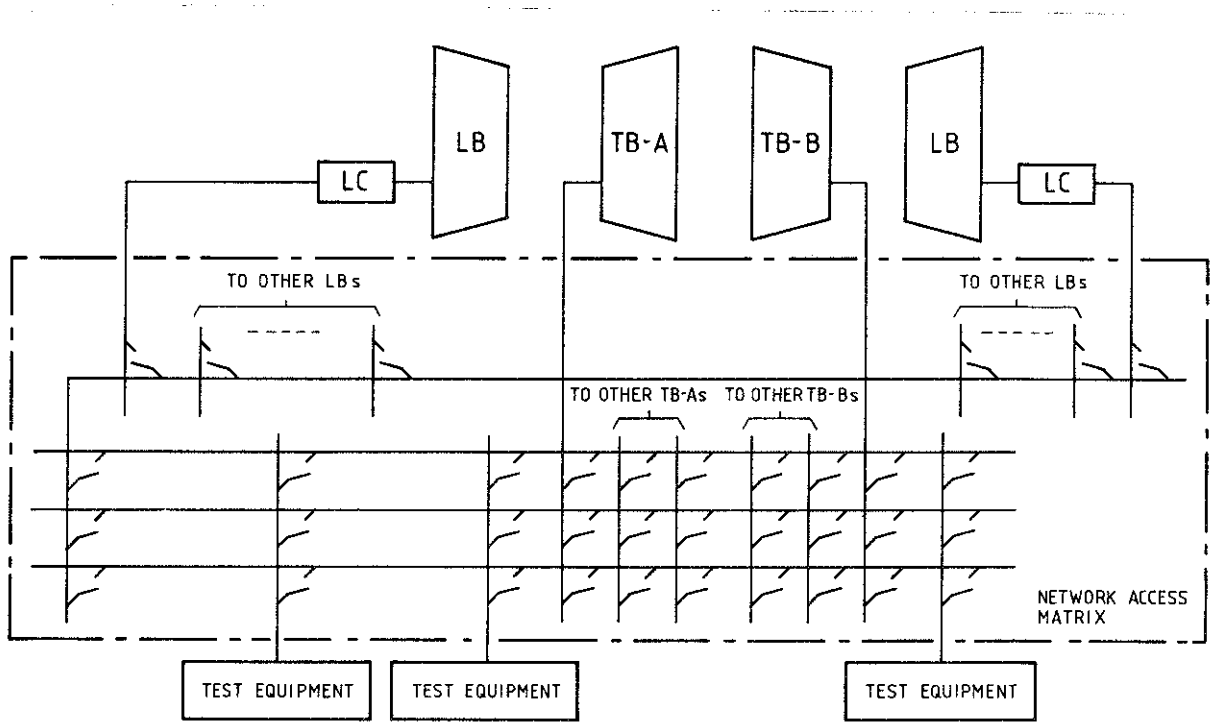

Fig. 3.2. Simplified Diagram of The Test System

3.5. Power Supplies

The system is supplied with 48V/50V which is distributed from the exchange battery via feeder cables and busbars to the equipment cabinets. The lower voltages (5V, 12V, etc.) used by the electronic circuitry are obtained via DC/DC converters, normally consisting of two coupled printed wiring boards. In the cabinets containing the telephony subsystems, the power supply outputs are interconnected in parallel in such a manner that if one supply unit should fail, the others are capable of continuing the operation of the cabinets involved. Fuses are provided to protect wiring, connectors and printed wiring including the 5V distribution wiring for IC logic, if a short circuit to earth occurs.

To avoid loss of information due to mains power failure, a power guarding facility is provided in each processor. This facility is activated if the primary voltage drops below a certain value and then the processor is brought to a controlled halt condition. This inhibits the memory read and write activities so that the memory contents cannot be corrupted. The Central Memory is guarded by the power guarding facility of the main processor.